WHAT IS CLAIMED IS:

1.   An input/output node switch for a multiprocessor computer system, said input/output node switch comprising:

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        a bridge unit implemented on an integrated circuit chip coupled to receive a plurality of peripheral transactions from a peripheral bus and configured to transmit a plurality of upstream packet transactions corresponding to said plurality of peripheral transactions;

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        a packet bus switch unit implemented on said integrated circuit chip coupled to receive said plurality of upstream packet transactions on an internal point-to-point packet bus link and configured to determine a destination of each of said plurality of upstream packet transactions;

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        wherein said packet bus switch unit is further configured to route selected ones of said plurality of upstream packet transactions to a first processor interface coupled to a first point-to-point packet bus link and to route others of said plurality of upstream packet transactions to a second processor interface

20   coupled to a second point-to-point packet bus link in response to determining said destination each of said plurality of upstream packet transactions.

2.   The input/output node switch as recited in claim 1 further comprising a first

25 transceiver unit coupled to receive said selected ones of said of said plurality of upstream packet transactions and to transmit said selected ones of said of said plurality of upstream packet transactions on said first point to point packet bus link.

3.   The input/output node switch as recited in claim 2 further comprising a second transceiver unit coupled to receive said others of said plurality of upstream packet transactions and to transmit said others of said of said plurality of upstream packet transactions on said second point-to-point packet bus link.

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4.   The input/output node switch as recited in claim 3, wherein said packet bus switch unit is further configured to decode an address associated with each of said plurality of upstream packet transactions.

10   5.   The input/output node switch as recited in claim 4, wherein said packet bus switch unit is further configured to block additional ones of said plurality of upstream packet transactions dependent upon said address.

6.   The input/output node switch as recited in claim 5 further comprising a third

15   transceiver unit coupled to receive said additional ones of said plurality of packet transactions dependent upon said address and to transmit said packet transactions on a third point-to-point packet bus link to another node.

7.   The input/output node switch as recited in claim 6, wherein said third transceiver

20   unit is further configured to receive a second plurality of upstream packet transactions on said third point-to-point packet bus link and to transmit said second plurality of upstream packet transactions to said packet bus switch.

8.   The input/output node switch as recited in claim 7, wherein said packet bus switch

25   unit is further configured to decode an address associated with each of said second plurality of upstream packet transactions, to route selected ones of said second plurality of upstream packet transactions to said first processor interface coupled to said first point-to-point packet bus link and to route others of said plurality of upstream packet transactions

to said second processor interface coupled to said second point-to-point packet bus link dependent upon said address associated with each of said second plurality of upstream packet transactions.

5   9.   The input/output node switch as recited in claim 3, wherein said packet bus switch unit is further configured to receive a first plurality of downstream packet transactions sent by said first processor interface and a second plurality of downstream packet transactions sent by said second processor interface.

10   10.   The input/output node switch as recited in claim 9, wherein said packet bus switch unit is further configured to arbitrate between said first plurality of downstream packet transactions and said second plurality of downstream packet transactions.

   11.   The input/output node switch as recited in claim 10, wherein said packet bus

15 switch unit is further configured to route said first plurality of downstream packet transactions and said second plurality of downstream packet transactions to said first internal point-to-point packet bus link.

   12.   The input/output node switch as recited in claim 11, wherein said bridge unit is

20 further configured to decode an address of each of said first and said second plurality of downstream packet transactions and to initiate bus cycles corresponding to selected ones of said first and said second plurality of downstream packet transactions dependent upon said address.

25   13.   The input/output node switch as recited in claim 1, wherein said packet bus switch unit is further configured to determine said destination of each of said plurality of upstream packet transactions using a programmable look up table.

14.   The input/output node switch as recited in claim 3, wherein said packet bus switch unit is further configured to determine said destination of each of said plurality of upstream packet transactions using available buffer space counts corresponding to upstream devices coupled to said first and said second external packet bus links.

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15.   The input/output node switch as recited in claim 3, wherein said first, said second and said third point-to-point packet bus links are HyperTransport™ links each including a first set of uni-directional wires and a second set of uni-directional wires each configured to convey packets including control packets and data packets, wherein said control

10   packets include command packets, info packets and response packets and wherein said control packets and data packets share the same wires.

16.   A multiprocessor computer system comprising:

15   a first processor and a second processor each configured to execute programmed instructions;

        an input/output node switch implemented on an integrated circuit chip coupled to

20   said first processor by a first point-to-point packet bus link and coupled to said second processor by a second point-to-point packet bus link, wherein said input/output node switch includes:

            a bridge unit coupled to receive a plurality of peripheral transactions from

25   a peripheral bus and configured to transmit a plurality of upstream packet transactions corresponding to said plurality of peripheral transactions;

a packet bus switch unit coupled to receive said plurality of upstream packet transactions on an internal point-to-point packet bus link and configured to determine a destination of each of said plurality of upstream packet transactions;

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wherein said packet bus switch unit is further configured to route selected ones of said plurality of upstream packet transactions to a said first processor via said first point-to-point packet bus link and to route others of said plurality of upstream packet transactions to said second processor via said second point-to-point packet bus link in response to determining said destination each of said plurality of upstream packet transactions.

17. The computer system as recited in claim 16, wherein said input/output node switch further comprising a first transceiver unit coupled to receive said selected ones of said of said plurality of upstream packet transactions and to transmit said selected ones of said of said plurality of upstream packet transactions on said first point to point packet bus link.

18. The computer system as recited in claim 16, wherein said input/output node switch further comprising a second transceiver unit coupled to receive said others of said plurality of upstream packet transactions and to transmit said others of said of said plurality of upstream packet transactions on said second point-to-point packet bus link.

19. The computer system as recited in claim 16, wherein said packet bus switch unit is further configured to decode an address associated with each of said plurality of upstream packet transactions.

20.   The computer system as recited in claim 19, wherein said packet bus switch unit is further configured to block additional ones of said plurality of upstream packet transactions dependent upon said address.

5   21.   The computer system as recited in claim 20, wherein said input/output node switch further comprising a third transceiver unit coupled to receive said additional ones of said plurality of packet transactions dependent upon said address and to transmit said packet transactions on a third point-to-point packet bus link to another node.

10   22.   The computer system as recited in claim 21, wherein said third transceiver unit is further configured to receive a second plurality of upstream packet transactions on said third point-to-point packet bus link and to transmit said second plurality of upstream packet transactions to said packet bus switch.

15   23.   The computer system as recited in claim 22, wherein said packet bus switch unit is further configured to decode an address associated with each of said second plurality of upstream packet transactions, to route selected ones of said second plurality of upstream packet transactions to said first processor coupled to said first point-to-point packet bus link and to route others of said plurality of upstream packet transactions to said second
20   processor coupled to said second point-to-point packet bus link dependent upon said address associated with each of said second plurality of upstream packet transactions.

24.   The computer system as recited in claim 18, wherein said packet bus switch unit is further configured to receive a first plurality of downstream packet transactions sent by
25   said first processor and a second plurality of downstream packet transactions sent by said second processor.

25.   The computer system as recited in claim 24, wherein said packet bus switch unit is further configured to arbitrate between said first plurality of downstream packet transactions and said second plurality of downstream packet transactions.

5   26.   The computer system as recited in claim 25, wherein said packet bus switch unit is further configured to route said first plurality of downstream packet transactions and said second plurality of downstream packet transactions to said first internal point-to-point packet bus link.

10   27.   The computer system as recited in claim 26, wherein said bridge unit is further configured to decode an address of each of said first and said second plurality of downstream packet transactions and to initiate bus cycles corresponding to selected ones of said first and said second plurality of downstream packet transactions dependent upon said address.

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28.   The computer system as recited in claim 16, wherein said packet bus switch unit is further configured to determine said destination of each of said plurality of upstream packet transactions using a programmable look up table.

20   29.   The computer system as recited in claim 16, wherein said packet bus switch unit is further configured to determine said destination of each of said plurality of upstream packet transactions using an available buffer space count corresponding to each of said first processor and to said second processor.

25   30.   The computer system as recited in claim 16, wherein said packet bus switch unit is further configured to route each of said plurality of upstream packet transactions to a given processor having a higher available buffer space count.

31.   The computer system as recited in claim 21, wherein said first, said second and said third point-to-point packet bus links are HyperTransport™ links each including a first set of uni-directional wires and a second set of uni-directional wires each configured to convey packets including control packets and data packets, wherein said control

5   packets include command packets, info packets and response packets and wherein said control packets and data packets share the same wires.

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